SYLLABUS

1. **Course name:** Digital Systems
2. **Course code:** DIGI330163
3. **Credits:** 3 (3/0/6)

   Duration: 15 weeks (45h main course and 90h self-study)
4. **Instructors:**

   1- Nguyen Thanh Hai, PhD
   2- Nguyen Truong Duy, MEng
   3- Nguyen Duy Thao, MEng
   4- Nguyen Manh Hung, PhD
   5- Vo Duc Dung, MEng
5. **Course conditions**

   Prerequisites: Basic electronics
   Corequisites: N/A
6. **Course description**

This course provides students the knowledge of the numerical systems, the basic logic gates, and the fundamental theorems of Boolean algebra. In addition, students will learn the structure and operation of the TTL and CMOS families, the characteristics of digital ICs, the principle of converting between analog and digital signals, structure and operations of the memory ICs, the principle of digital oscillators. Finally, the course provides students how to calculate, identify combinational circuits, sequential circuits and solve the problems of the circuit, and then design digital systems.

7. **Course Goals**

Goals	***Goal description*** *(This course provides students:)*	**ELOs**
G1	Basic knowledge of digital systems.	01 (H)
G2	An ability to use textbooks, books, powerpoint slides and to do homeworks and exams in English.	05 (M)
G3	An ability to use tools and methods for solving problems related to digital systems.	07 (H)
G4	An ability to calculate and design digital circuits.	02 (H)

** Note: High: H; Medium: M; Low: L*

8. Course Learning Outcomes (CLOs)

CLOs		***Description*** *(After completing this course, students can have:)*	**Outcome**
G1	G1.1	The ability to apply the numeral systems and codes.	01 07
	G1.2	The ability to apply the logic gates, Flip-Flops and MSI ICs.	01 07
	G1.3	The ability to present the structure of memory and analog-to-digital conversion circuits.	01
G2	G2.1	The ability to read datasheets of digital ICs and lectures in English.	05
G3	G3.1	The ability to apply Boolean algebra, De-Morgan theorem, and K-map to simplify logic circuits.	01 07
	G3.2	The ability to use methods for designing the combinational logic circuits and the sequential logic circuits.	07
G4	G4.1	The ability to design and calculate for combinational logic circuits, sequential logic circuits, square oscillator, and timer circuits.	02
	G4.2	The ability to calculate for interfacing TTLs with CMOSs and digital ICs with power loads.	02 07
	G4.3	The ability to design for expansion of the digital IC's inputs/outputs.	02

9. Study materials

- Textbooks:

[1] Nguyen Đinh Phu, Nguyen Truong Duy, *Giao trinh ky thuat so*, VNU-HCMC Publishers, 2012.

- References:

[1] Nguyen Huu Phuong, *Mach So*, Thong Ke Publishers, 2004.

[2] Ronald J. Tocci, *Digital systems*, tenth edition, Prentice Hall 2010.

10. Student Assessments

- Grading points: 10
- Planning for students assessment is followed:

Type	**Contents**	**Linetime**	**Assessment techniques**	**CLOs**	**Rates (%)**
Midterms					**50**
Exam01	- Combination logic circuits. - Multiplexer and Demultiplexer. - Encoder and Decoder.	Week 10	Individual paper assessment in class	G1.2, G3.1 G4.1, G4.3	30
Exam02	- Count systems and codes. - Boolean algebra and logic gates. - Binary adder and subtractor	week 12	Online test Quiz	G1.1 G2.1 G3.1	10

	circuits. - Binary conparator. - Integrated circuit technology.			G4.2	
Exam03	- Design and simulation of an application circuits.	weeks 6-14	Topic	G1.2, G1.3 G2.1, G3.2 G4.2, G4.3	10
Final exam					**50**
Final Exam	- Sequential logic circuits – Flip-Flop. - Counters and/or Registers. - Oscillators and timers. - Memory devices. - ADC or/and DAC.		Individual paper assessment in class	G1.2 G1.3 G2.1 G3.2 G4.1	50

11. Course details:

Weeks	Contents	CLOs
1	***Chapter 1:*** **<NUMBER SYSTEMS AND CODES>** *(3/0/6)*	
	A/ **Contents and teaching methods***: (3)* **Contents:** 1.1 Digital and analog systems. 1.2 Number systems. 1.3 Conversion between different number systems. 1.4 Computational methods in binary. 1.5 Computational methods in Hexadecimal. 1.6 Codes. **Teaching methods**: + Traditional lectures using powerpoint to review basic knowledges of steel structures course, to demonstrate large applications of these structures in different buidings. A series of diagnostic questions will be also used to estimate students knowledges. + Questions.	G1.1 G2.1
	B/ **Self-study contents**: *(6)* + ASCII code, complement systems, exceed 3 code. + Exercises and homeworks.	G1.1
2	***Chapter 2:*** **<BOOLEAN ALGEBRA AND LOGIC GATES>** *(3/0/6)*	
	A/ **Contents and teaching methods***: (3)* **Contents:** 2.1 Boolean algebra. 2.2 Logic gates. 2.3 Conversion method and logic gates.	G1.1 G1.2 G2.1 G3.1 G4.1

	2.4 Karnaugh map method. 2.5 Combinational logic circuits design. 2.6 Examples and Exercises. **Teaching methods**: + Theoretical lectures. + Questions.	
	***B/* Self-study contents**: *(6)* + Construction of three-inputs logic gates AND, OR, NAND, NOR, EXOR, EXNOR from two-inputs NAND and NOR gates. + Exercises.	G1.1 G1.2 G4.1
3	***Chapter 3:* <SEQUENTIAL CIRCUITS _ FLIP-FLOP>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** 3.1 Introduction to sequential circuits. 3.2 NAND and NOR gate latches. 3.3 Types of Flip-Flops. 3.4 Flip-Flop conversion methods. **Teaching methods**: + Theoretical lectures. + Questions.	G1.2 G2.1
	***B/* Self- study contents**: *(6)* + Setting a truth table for Flip-Flops. + Conversion of Flip-Flops from one Flip-Flop to another. + Exercises.	G1.2
4	***Chapter 4:* <COUNTERS AND SHIFT REGISTERS>** *(6/0/12)*	
	A/* Contents and teaching methods: (3)* **Contents:** 4.1 Introduction. 4.2 Asynchronous counters. 4.3 Mod 2^n counter circuits. 4.4 Mod N counter circuits. 4.5 Preset state for counter. **Teaching methods**: + Theoretical lectures. + Question.	G1.1 G1.2 G2.1 G3.2 G4.1
	***B/* Self- study contents**: *(6)* + Design of Mod counters. + Exercises.	G3.2 G4.1
5	***Chapter 4:* <COUNTERS AND SHIFT REGISTERS (cont.)>** *(6/0/12)*	

	A/* Contents and teaching methods: (3)* **Contents:** 4.6 Synchronous counters. 4.7 Ring counters. 4.8 Johnson counters. 4.9 Shift registers. **Teaching methods**: + Theoretical lectures. + Questions.	G1.2 G2.1 G3.2 G4.1
	***B/* Self- study contents**: *(6)* + Design of various synchronous counters and shift registers. + Exercises.	G4.1
6	***Chapter 5:* <INTEGRATED CIRCUIT TECHNOLOGIES>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** 5.1 TTL circuits. 5.2 CMOS circuits. 5.3 TTL and CMOS interface. 5.4 Logic gates and load interface. **Teaching methods**: + Theoretical lectures. + Questions.	G2.1 G4.2
	***B/* Self- study contents**: *(6)* + How to use IC's datasheet. + Exercises.	G2.1
7	***Chapter 6:* <MSI LOGIC CIRCUITS>** *(9/0/18)*	
	A/* Contents and teaching methods:(3)* **Contents:** 6.1 Encoders. 6.2 Decoders. 6.3 BCD-to-7-segment decoder. **Teaching methods**: + Theoretical lectures. + Questions.	G1.2 G2.1 G3.2 G4.1
	***B/* Self- study contents**: *(6)* + Design of BCD-to-7-segment cathode led decoder. + Transcoding circuits. + Exercises.	G4.1
8	***Chapter 6:* <MSI LOGIC CIRCUITS (cont.)>** *(9/0/18)*	

	A/* Contents and teaching methods: (3)* **Contents:** 6.4 Multiplexers. 6.5 Demultiplexers. 6.6 Expansion methods of inputs/outputs for encoders, decoders, multiplexers and demultiplexers. **Teaching methods**: + Theoretical lectures. + Questions.	G1.2 G2.1 G3.2 G4.1 G4.3
	***B/* Self- study contents**: *(6)* + Design of multiplexers and demultiplexers. + Expansion inputs/outputs for multiplexers and demultiplexers. + Exercises.	G3.2 G4.1 G4.3
9	***Chapter 6:* <MSI LOGIC CIRCUITS (cont.)>** *(9/0/18)*	
	A/* Contents and teaching methods: (3)* **Contents:** 6.7 Binary adder and subtractor. 6.8 Binary comparator. 6.9 Parity method for error detection. **Teaching methods**: + Theoretical lectures. + Questions.	G1.1 G1.2 G2.1 G4.1
	***B/* Self- study contents**: *(6)* + BCD adder and binary multiplier. + Exercises.	G4.1 G4.3
10	**<EXERCISES AND TESTS>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** + Homeworks. + Exam-1. **Teaching methods**: + Questions and answers. + Guide to do exercises.	G1.1 G1.2 G2.1 G3.1 G4.1
	***B/* Self- study contents**: *(6)* + Reinforce the knowledge learned.	G4.1 G4.3
11	***Chapter 7:* <DIGITAL OSCILLATORS AND TIMERS>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** 7.1 Introduction. 7.2 Oscillators and timers using logic gates.	G1.2 G2.1 G4.1

	7.3 Introduction to an IC 555 timer. 7.4 Oscillators and timers using IC 555. **Teaching methods**: + Theoretical lectures. + Questions.	
	***B/* Self- study contents**: *(6)* + Analysis of the operation of the Oscillators and timers using logic gates and IC 555. + Exercises.	G1.2
12	**<PRESENTATION TOPIC>**	
	A/* Contents and teaching methods: (3)* **Contents:** + Students presented the report in groups. **Teaching methods**: + Questions. + Discuss.	G1.2 G1.3 G2.1 G3.2 G4.2 G4.3
	***B/* Self- study contents**: *(6)* + Complete report presentation.	
13	***Chapter 8:* <MEMORY DEVICES>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** 8.1 Introduction. 8.2 Types of memory devices. 8.3 Capacity Expansion of memory. **Teaching methods**: + Theoretical lectures. + Questions.	G1.3 G2.1 G4.3
	***B/* Self- study contents**: *(6)* + How to use Proteus software and simulation circuits using EPROM. + Homeworks.	G4.3
14	***Chapter 9:* <DIGITAL ANALOG CONVERSION>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** 9.1 Introduction of DAC and ADC. 9.2 Types of DAC. 9.3 Types of ADC. **Teaching methods**: + Theoretical lectures. + Question.	G1.3 G2.1

	***B/* Self- study contents**: *(6)* + Analysis of the operation of the DAC and ADC. + Homeworks.	G1.3
15	**<REVIEW>** *(3/0/6)*	
	A/* Contents and teaching methods: (3)* **Contents:** + Review contents. + Exercises. **Teaching methods**: + Questions and answers. + Instructing to do exercises.	G1.2, G1.4, G2.1, G3.1, G3.2, G4.1, G4.2, G4.3
	***B/* Self- study contents**: *(6)* + Reinforce the knowledge learned. + Exercises.	G1.2, G1.4, G2.1, G3.1, G3.2, G4.1, G4.2, G4.3

12. Learning ethics:

Home assignments and projects must be done by the students themselves. Plagiarism found in the assessments will get zero point.

13. First approved date: August 1st 2012

14. Approval level:

Dean **Department** **Instructor**

15. Syllabus updated process

1st time: Updated content dated, **August 1st 2014**	Instructors Head of department
2nd time: Updated content dated, **August 1st 2016**	Instructors Head of department